T2: Design and test of 3D-IC

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- **Abstract**

In this talk, we will discuss the Through Silicon Via (TSV) based 3D-IC design and research on 3D-IC heterogeneous integration of wireless sensor node. Emerging as a mainstream integration technology, the 3D-IC design goes beyond the traditional 2D-IC design methodology and extends to include new design methods and techniques to tackle the challenges and issues introduced by the TSV-based die stacking. In the coming More-Than-Moore era, TSV-based 3D-IC design is expected to continue the integration advancement not by device size shrinking but vertical stacking at lower cost, ideally for sensor node based heterogeneous Internet-of-Thing (IoT) applications. The involution to 3D-IC design by extending the traditional design methodology to the TSV-based integration technology, poses new challenges in achieving high design efficiency and productivity, while maintaining minimized design complexity and effort. In the talk, we will discuss the 3D-IC design, challenges and opportunities, and highlight some research on 3D heterogeneous integration from system architecture, design methodology, to the design for testability.

- **Biography: Dr. WANG, Chao**

Dr. Wang received his B.Eng. and PhD degrees, both in Electronic Engineering, from the Huazhong University of Science and Technology (HUST), Wuhan, China in 2000, and the Nanyang Technological University (NTU), Singapore in 2008, respectively. From 2005 to 2007, he was also with the Center for Signal Processing, NTU as a Research Engineer. He developed real-time embedded image/video surveillance systems. From 2008 to 2010, he worked as an IC Design Engineer with the Imaging Division, STMicroelectronics (STM), Asia-Pacific Headquarter, Singapore. As core designers, he participated in the development of STM 2/3/5 MPix Bayer/YUV CMOS image sensor and processor ICs for mobile camera applications. Currently, he is a Research Scientist with the Institute of Microelectronics (IME), Agency for Science, Technology and Research (A*STAR), Singapore. His research interests include energy-efficient SoC & VLSI design for biomedical, image, and video applications, ultra-low-voltage IC design, TSV-based 3D-IC design, and Design for Testability (DFT).