T1: Low-voltage and variation-tolerant design

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• Abstract

Ultra-low voltage operation (i.e. sub-threshold/near-threshold operation) has emerged as a promising technique to achieve highly energy-efficient SoCs. The circuit behavior at ultra-low voltages is significantly different from that in the super-threshold region. To enable ultra-low voltage operation, the standard cell library needs to be re-characterized with cell re-selection. Some critical cells (e.g. flip-flop, level shifter) need to be redesigned. In addition, some challenges come along with the benefit of energy reduction, such as performance degradation and increasing variability. In this talk, we will introduce the opportunities and challenges of the ultra-low voltage operation, show the design of some critical circuits for enabling ultra-low voltage operation, and discuss the techniques for addressing the variability issue at ultra-low voltages. We will also show some examples of ultra-low voltage SoC design.

• Biography: Dr. ZHOU, Jun

Dr. Zhou received Dual B.Eng. Degree in Communication Engineering and Microelectronics from University of Electronic Science and Technology of China, and Ph.D. degree in Microelectronics System Design from Newcastle University, UK, in 2004 and 2008 respectively. From 2008 to 2010, he worked as a research scientist in the Ultra-Low Power DSP Group, IMEC, Netherlands. He participated in several projects as core member to design ultra-low power DSP for Philips and NXP for wireless intelligent sensor applications. In 2011, he joined the Institute of Microelectronics (IME), Agency for Science, Technology and Research (A*STAR), Singapore, where he leads projects in energy-efficient and variation-tolerant VLSI design. He also co-supervises PhD students from National University of Singapore (NUS) and Nanyang Technological University (NTU). Dr. Zhou Jun has published over 20 papers in energy-efficient and variation-tolerant circuit and system design, including ISSCC, JSSC, TCASI, DAC and ASSCC.