Reliability Challenges for High Performance Electronics in the Internet of Things Era

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Outline

- ❑ Todays' electronics, and technological development till now.

- ❑ Reliability Challenges for today's electronics:

  - ➢↑ Vulnerability to transient faults (TFs) → soft errors (SEs)

  - ➢↑ Likelihood of Aging Phenomena (NBTI)

- ❑ Design Approaches for Reliable electronics.

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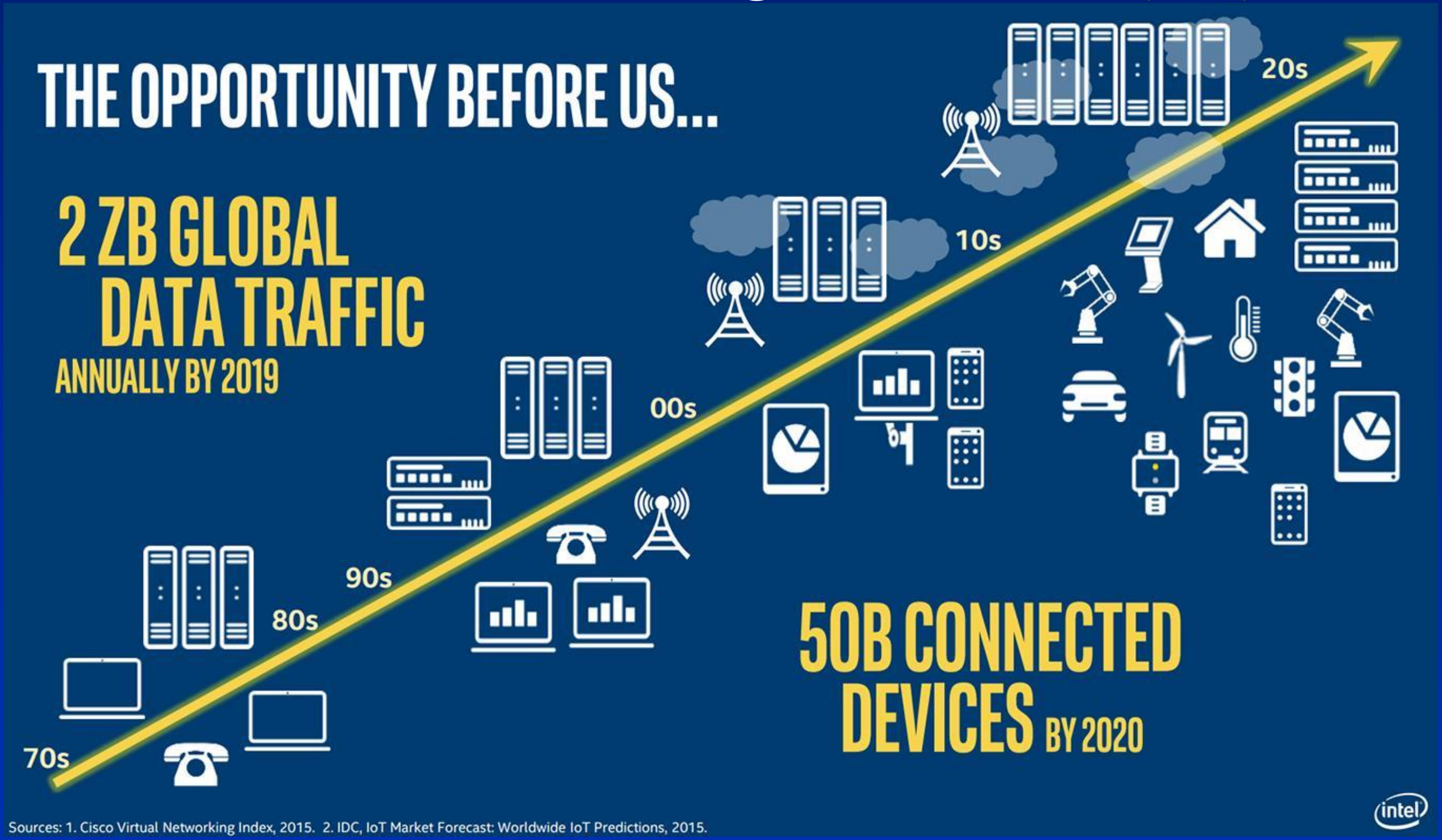
- ❑ Design Approaches for Reliable electronics.

Today’s Electronics

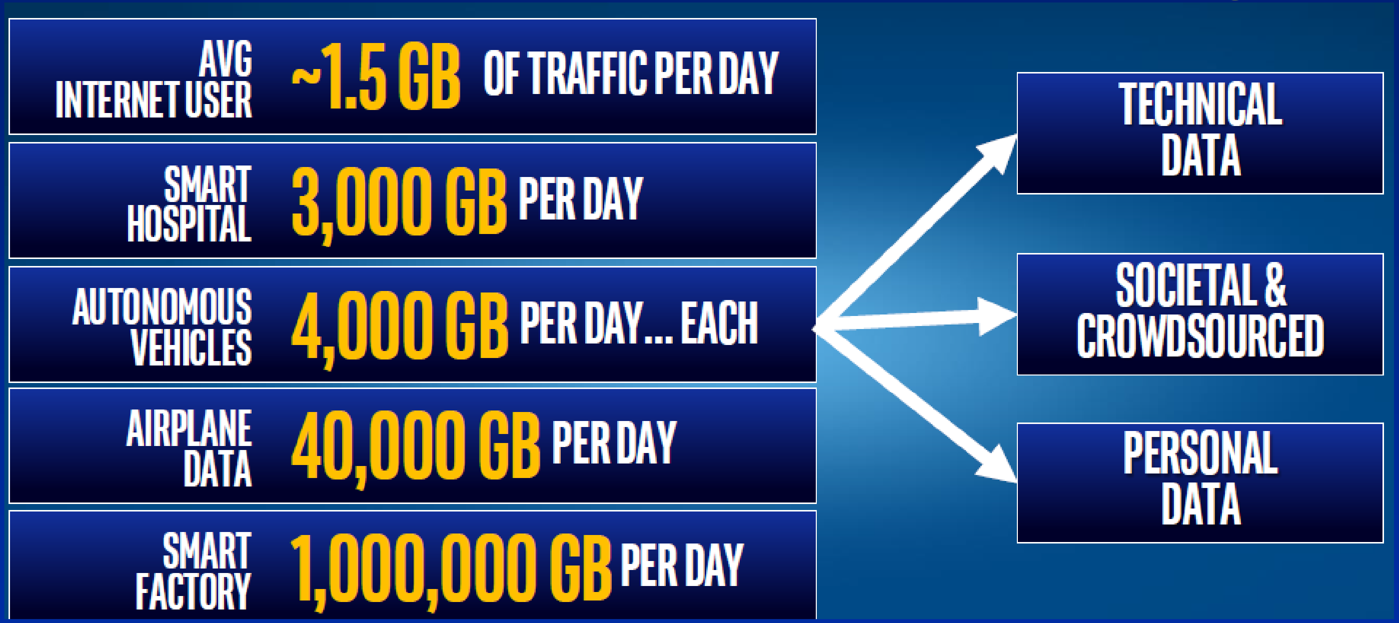
- ❑ Continuous miniaturization of microelectronic technology → massive diffusion/presence of electronic devices, possibly connected to each other through the Internet (IoT).



Sources: 1. Cisco Virtual Networking Index, 2015. 2. IDC, IoT Market Forecast: Worldwide IoT Predictions, 2015.

IoT, Big Data and Reliability

- ❑ Huge amount of electronic devices connected **through the Internet (IoT) → huge amount of data** to be **stored** (*Data Center/Cloud/Fog*), **processed** and **distributed again.**



AVG INTERNET USER ~1.5 GB OF TRAFFIC PER DAY

SMART HOSPITAL 3,000 GB PER DAY

AUTONOMOUS VEHICLES 4,000 GB PER DAY… EACH

AIRPLANE DATA 40,000 GB PER DAY

SMART FACTORY 1,000,000 GB PER DAY

TECHNICAL DATA

SOCIETAL & CROWDSOURCED

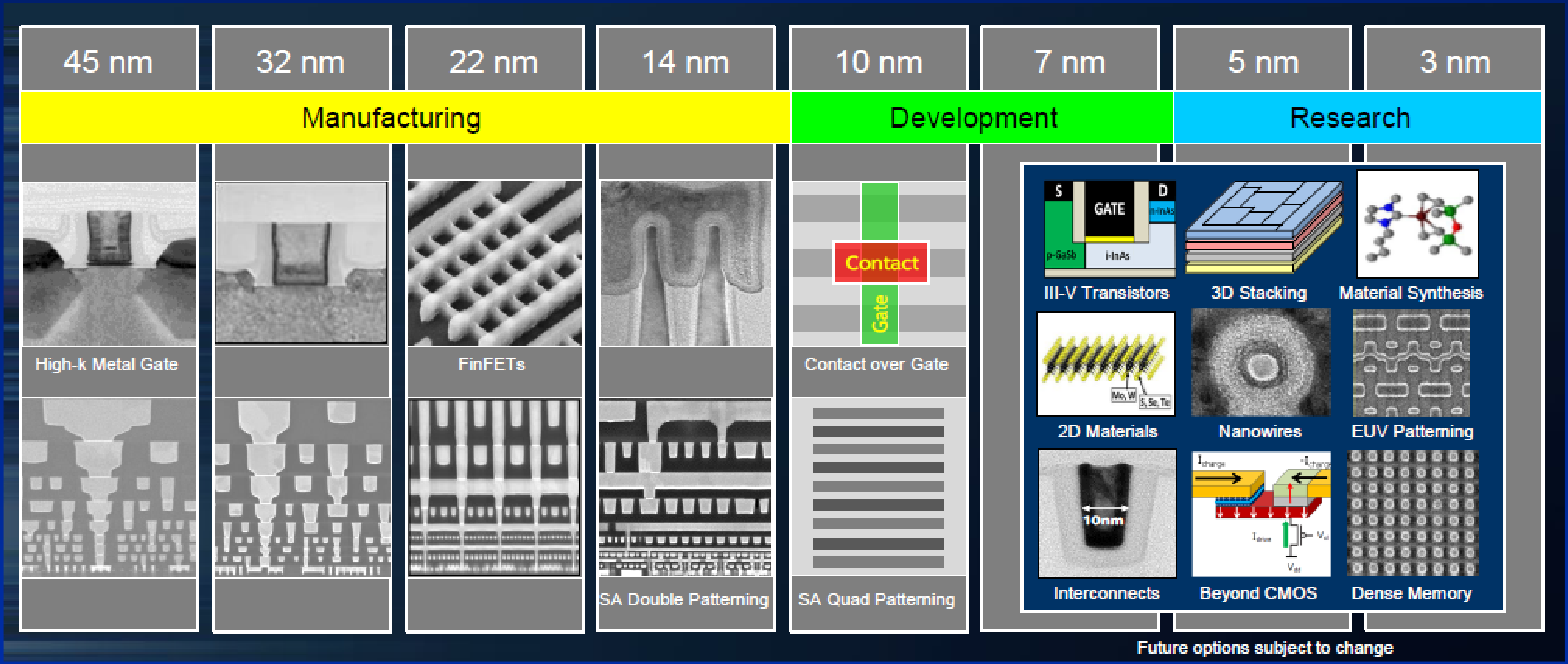
PERSONAL DATA

R. Mariani, "Making the Autonomous Dream Work", Intel Fellow, Unviersity of Bologna presentation, May 2018

- ❑ Life's **decisions driven by such data** (autonomous drive factory, transport, home, etc).

But can we rely on these data? Is the electronic storing/processing them reliable?

Today's Electronic Technology



45 nm | 32 nm | 22 nm | 14 nm | 10 nm | 7 nm | 5 nm | 3 nm

Manufacturing | Development | Research

High-k Metal Gate

FinFETs

Contact over Gate

SA Double Patterning

SA Quad Patterning

III-V Transistors

3D Stacking

Material Synthesis

2D Materials

Nanowires

EUV Patterning

Interconnects

Beyond CMOS

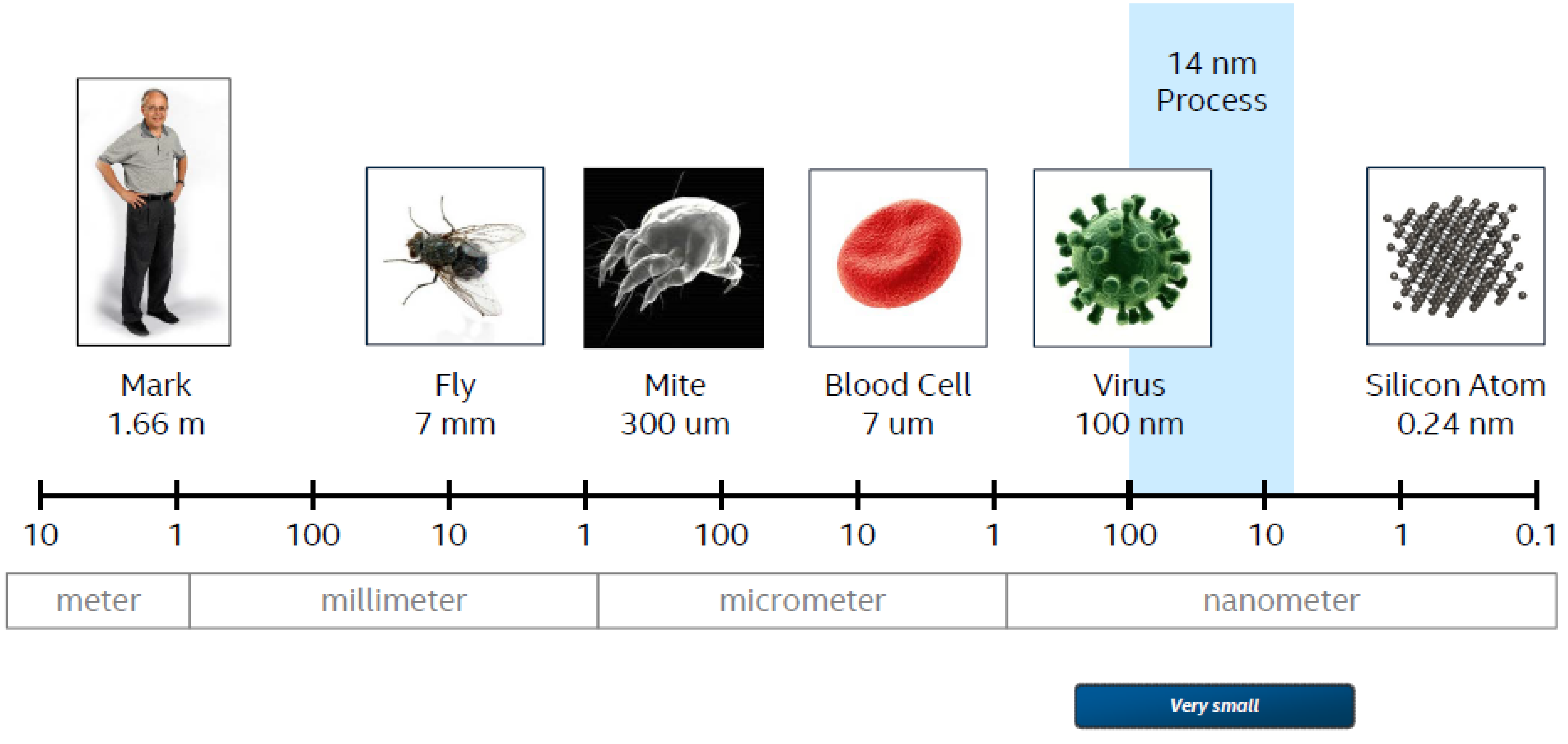
Dense Memory

Future options subject to change

M. Bohr, "Continuing Moore's Law", Technology and Manufacturing Day, 19 September 2017

Today’s Electronic Technology (cont’d)

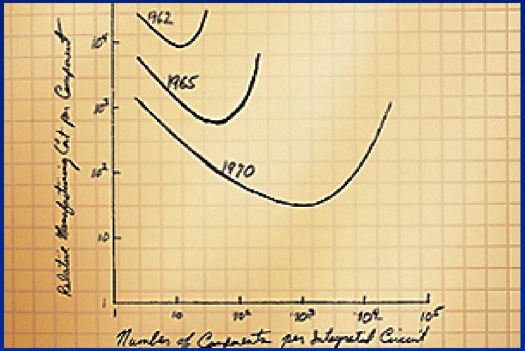
- How much small are 14nm?



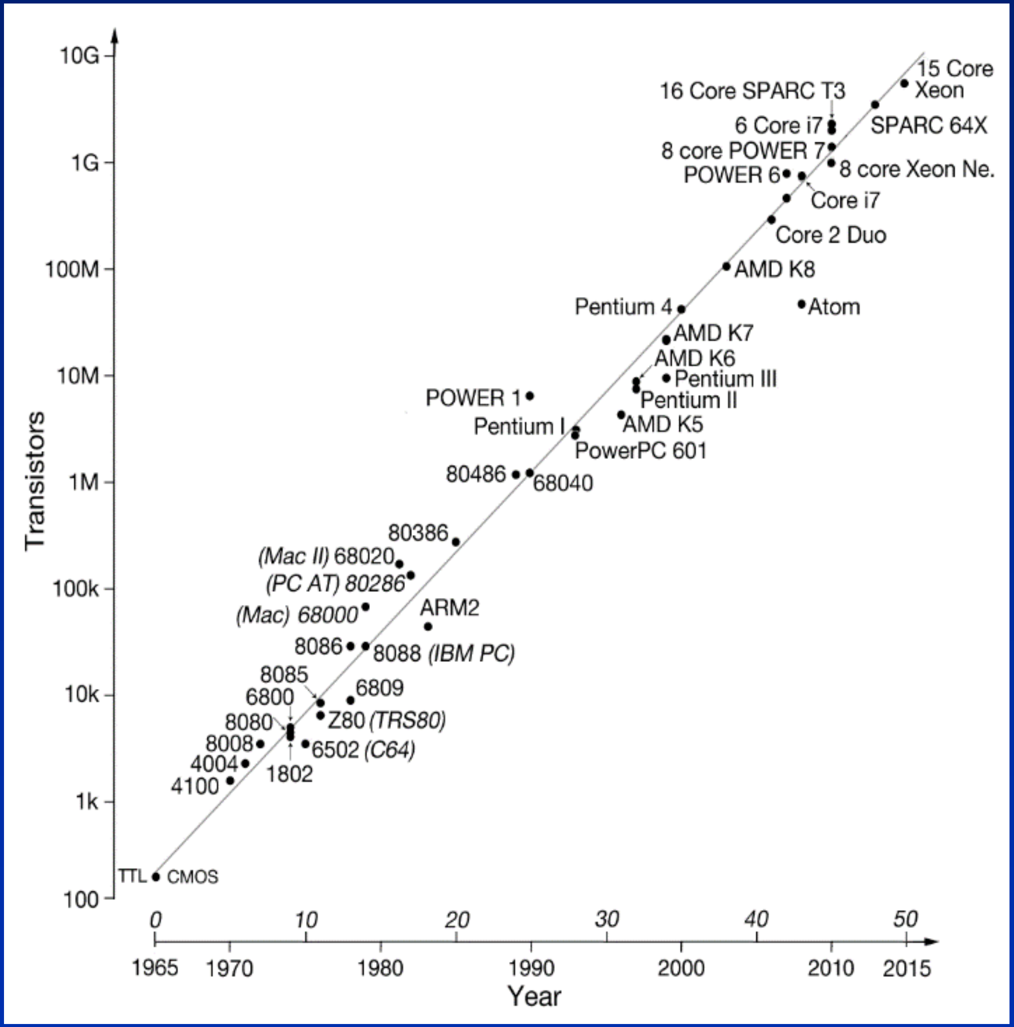
M. Bohr, “14nm Process Technology: Opening New Horizons ”, Intel Developer Forum, 2014

Development of Electronic Technology

- The Moore law (1965) has **driven the evolution of microelectronic technology** and is **driving its future developments.**



Courtesy of Intel Corporation
Intel Techn. Journal, 2007



https://www.elektormagazine.com/articles/moores-law

How Has It Been Possible to Follow the Moore's Law?

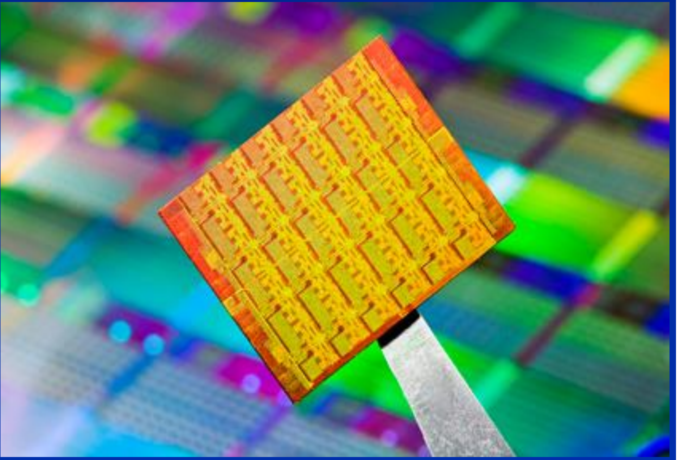
- ❑ **Architectural Changes: multicore/many-core systems (since 2000)**

- ❑ **Material Changes: high-k gate insulator (since 2007)**

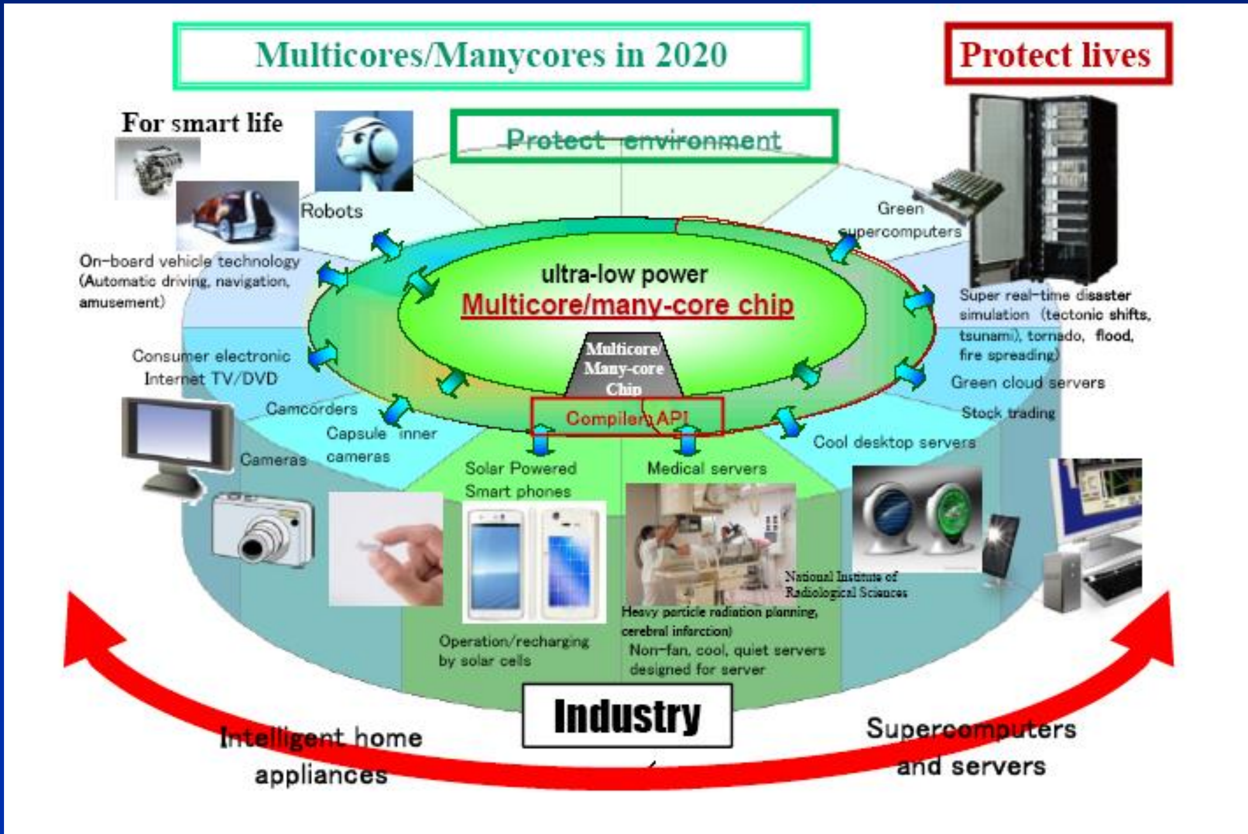
- ❑ **Device Changes: Tri-gate transistors (since 2011)**

How Has It Been Possible to Follow the Moore’s Law?

- ❑ **Architectural Changes:** **multicore/many-core systems (since 2000)**
  - ➢ **June 15, 2010: Experimental microprocessor with 48-cores**
  - ➢ **A trend that will continue**



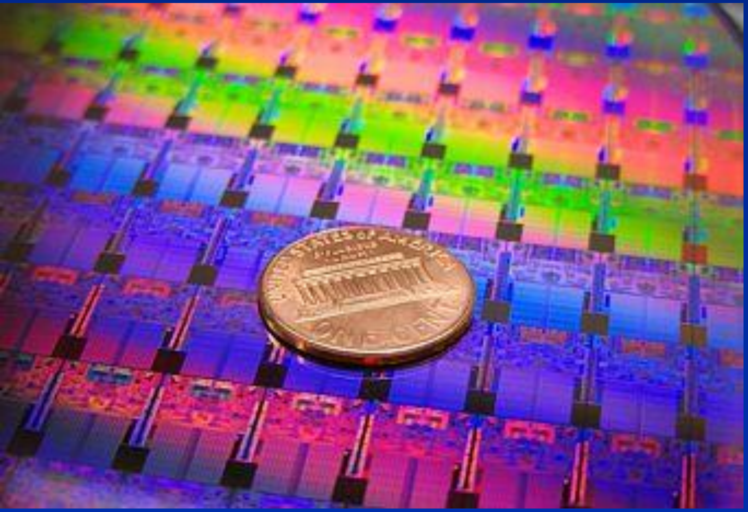
http://www.intel.com/pressroom/innovation, June 15, 2010

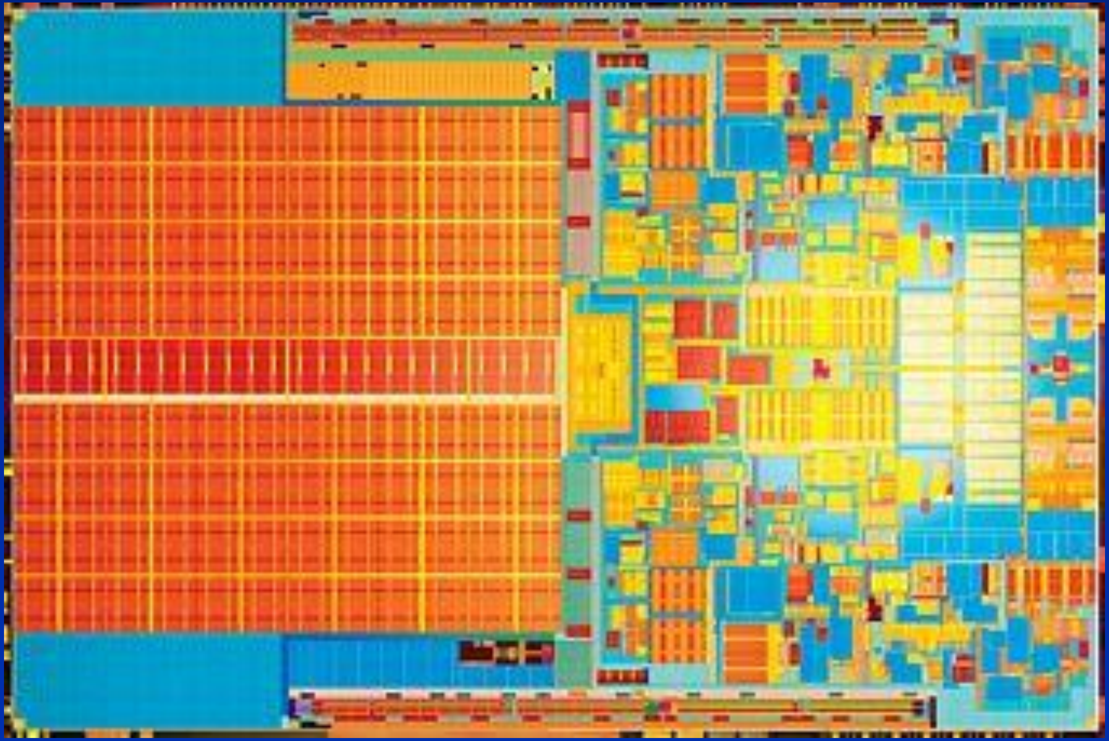

Multicores/Manycores in 2020
Protect lives
For smart life
Robots
Protect environment
Green supercomputers
On-board vehicle technology (Automatic driving, navigation, amusement)
ultra-low power
Multicore/many-core chip
Super real-time disaster simulation (tectonic shifts, tsunami), tornado, flood, fire spreading)
Multicore/ Many-core Chip
Consumer electronic Internet TV/DVD
Green cloud servers
Camcorders
Compiler API
Stock trading
Capsule inner cameras
Cameras
Cool desktop servers
Solar Powered Smart phones
Medical servers
National Institute of Radiological Sciences
Heavy particle radiation planning, cerebral infarction)
Operation/recharging by solar cells
Non-fan, cool, quiet servers designed for server
Industry
Intelligent home appliances
Supercomputers and servers

IEEE Computer Society 2022 Report, 2014

How Has It Been Possible To Follow the Moore Law? (cnt'd)

- ❑ **Material Changes: high-k gate insulator (since 2007)**
  - ➢ **Intel 45nm dual-core, Hafnium-based High-k Metal Gate process.**

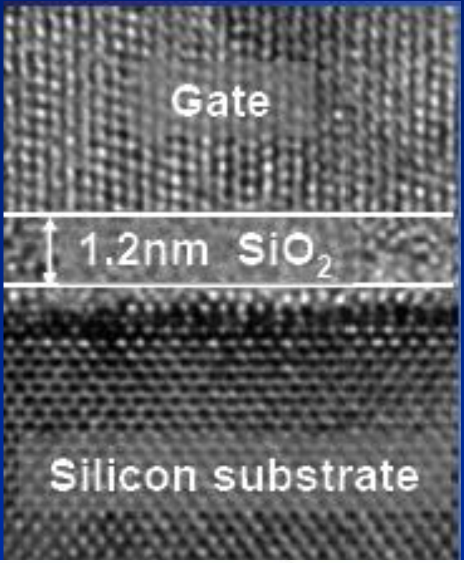


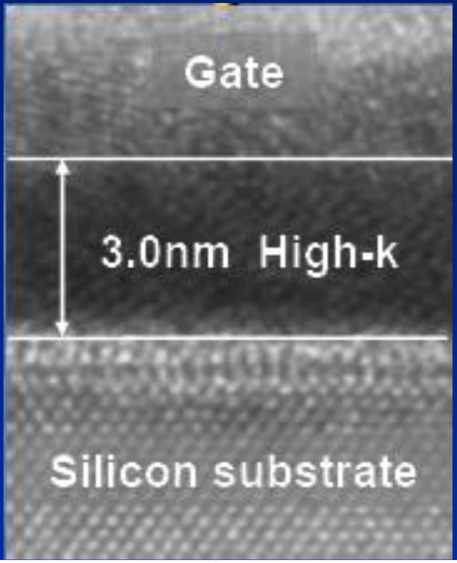


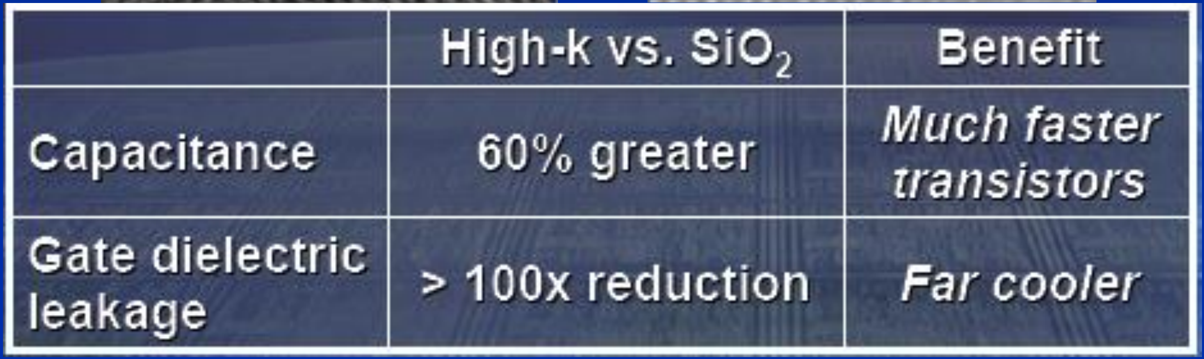
Intel Press Kit, November, 2007

How Has It Been Possible To Follow the Moore Law? (cnt'd)

❑ **Hafnium-based High-k Metal Gate process advantages:**





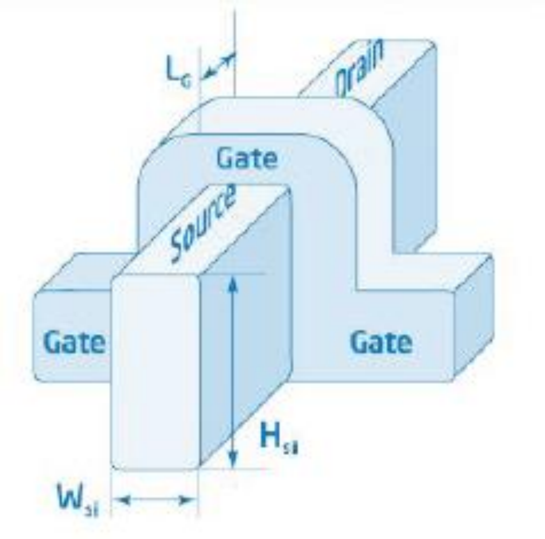


	High-k vs. SiO$_2$	Benefit
Capacitance	60% greater	*Much faster transistors*
Gate dielectric leakage	> 100x reduction	*Far cooler*

Intel's High-k/Metal Gate k/Metal Gate Announcement November 4th, 2003

How Has It Been Possible To Follow the Moore Law?(cnt'd)

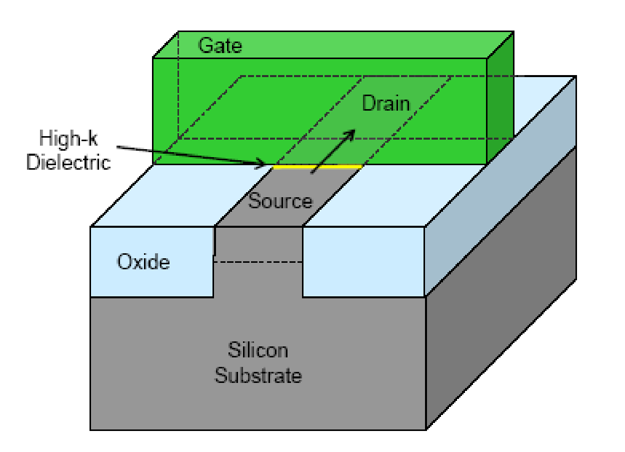
- ❑ **Device Changes: Tri-gate transistors (since 2011):**
  - ➢ **Tri-Gate Transistors → higher speed & lower I_{OFF} (→ low power consumption) [2002].**
    - ✓ **Tri-Gate Transistors used in 22nm SRAM demonstrated in 2009**
    - ✓ **Tri-Gate Transistors used in 22nm microprocessor demonstrated in April 2009**



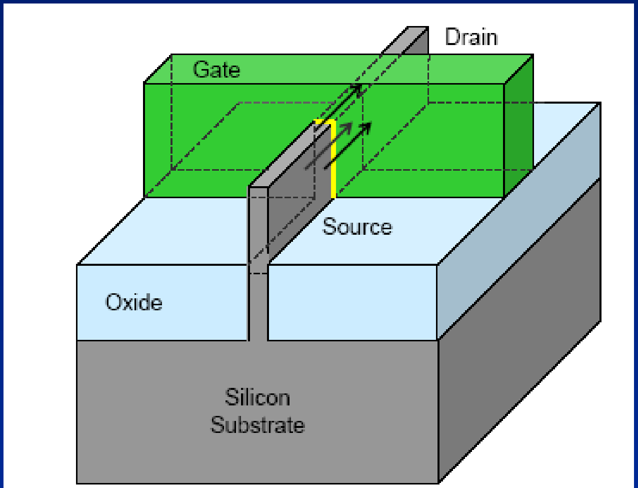
R. S. Chau, Technology @ Intel Magazine, August 2006

How Has It Been Possible To Follow the Moore Law? (cnt'd)

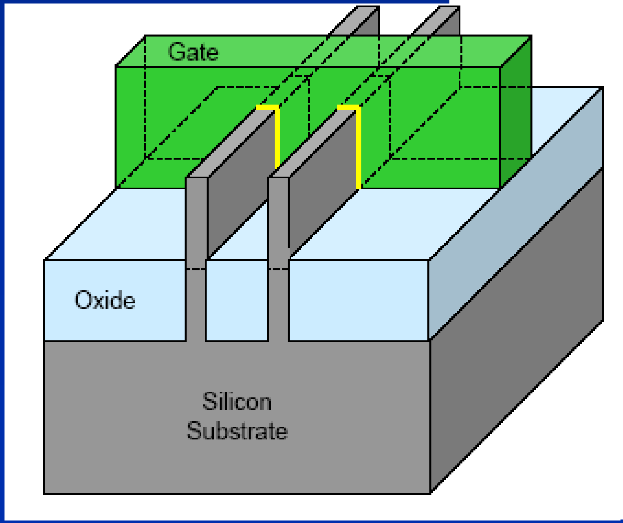
- ❑ Planar Transistor



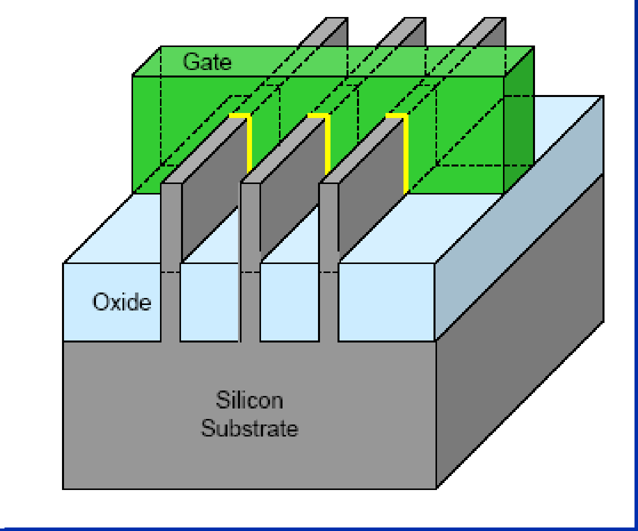
- ❑ Tri-Gate Transistor



- ➢ 2 fins



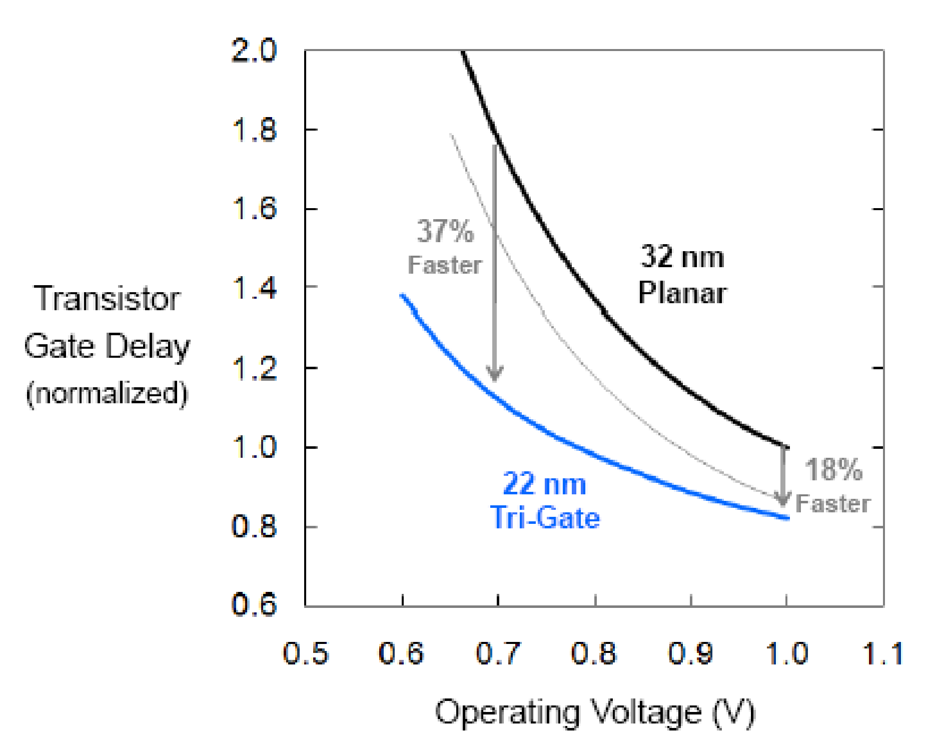
- ➢ 3 fins



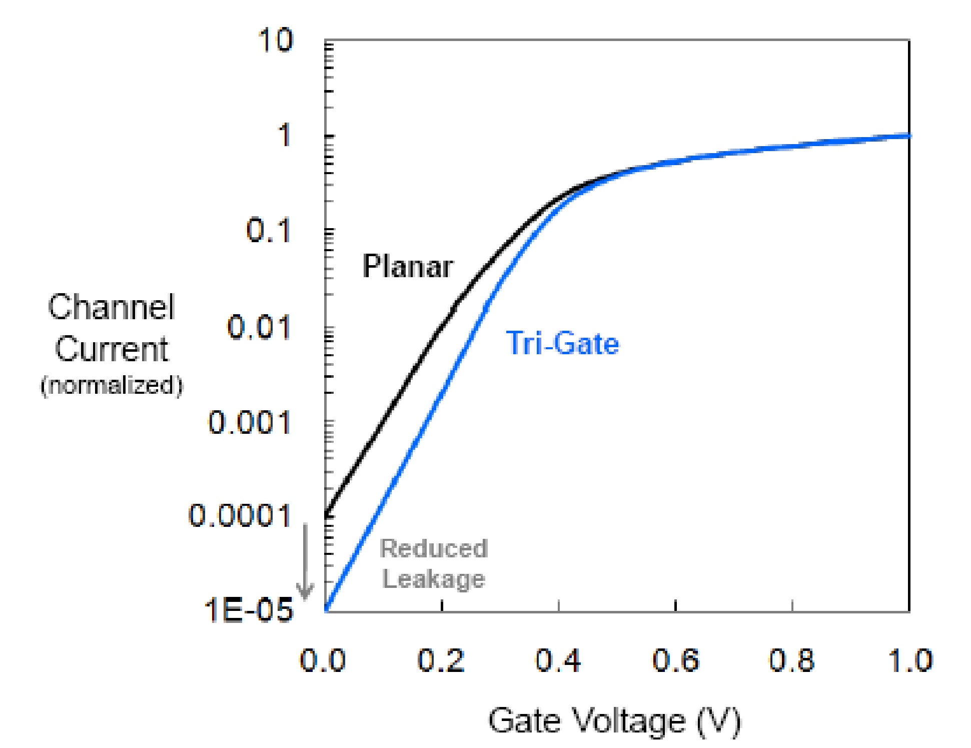
Bohr, Mistry, "22nm Details_Presentation", May 2011

How Has It Been Possible To Follow the Moore Law? (cnt'd)

❑ **Higher Speed**



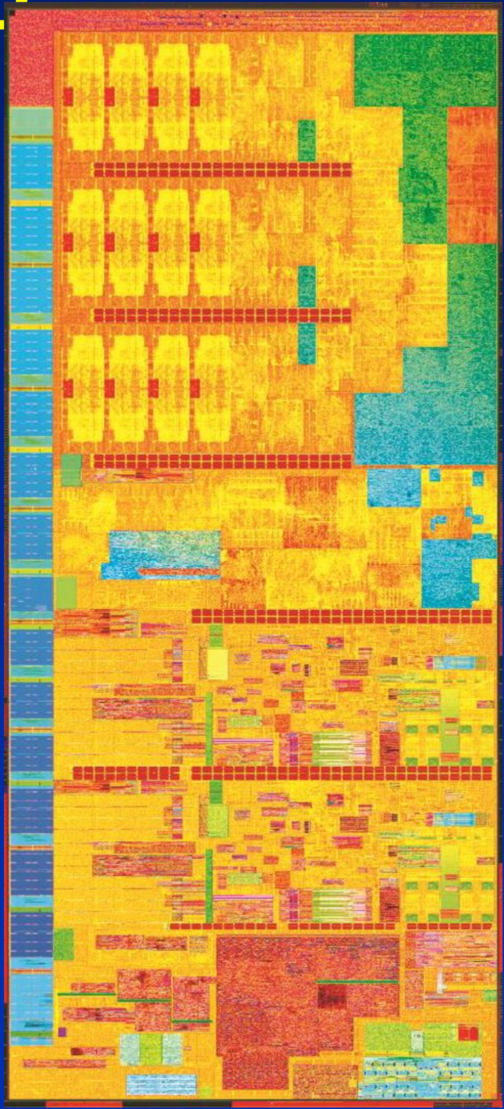
❑ **Reduced Leakage (I_{OFF})**



Bohr, Mistry, "22nm Details_Presentation", May 2011

How Has It Been Possible To Follow the Moore Law? (cnt'd)

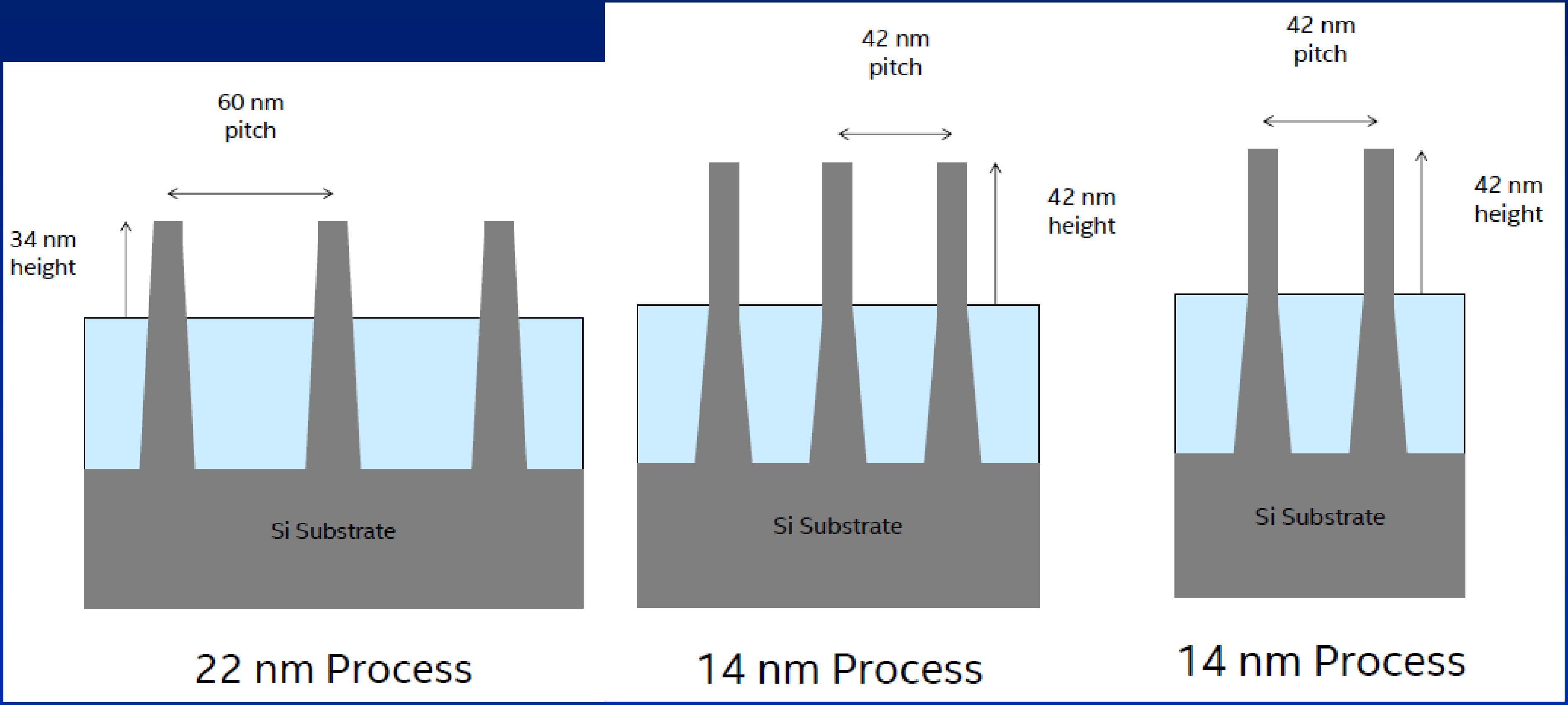
- Intel® Core™ M Processor (announced on September 5th, 2014):
  - 14 nm, 2nd generation 3-gate transistor technology
  - 1.3 billion transistors
  - Compared to previous Intel Core processors
    - ↑50% performance
    - ↑40% graphic elaboration speed
    - ↑20% autonomy of charge



Intel Developer Forum San Francisco 2014

How Has It Been Possible To Follow the Moore Law?(cnt'd)

2nd generation 3-gate transistors



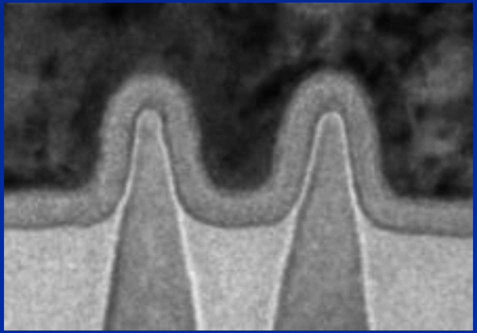
Intel Developer Forum San Francisco 2014

- ❑ **Closer fins → ↑ integration density**
- ❑ **Thinner and higer fins → ↑ performance**
- ❑ **Lower number of fins → ↑ integration density**

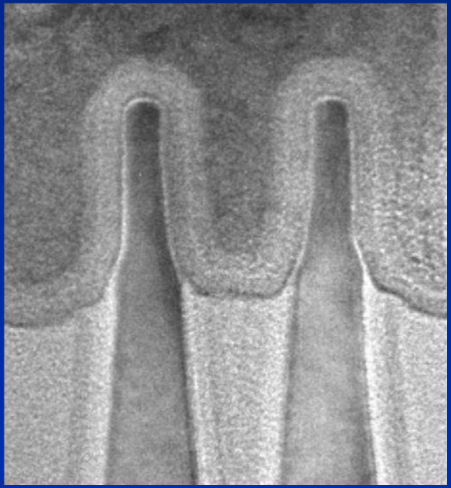
How Is It Possible To Follow the Moore Law?

- **10nm process using the 3^{rd} generation of 3-gate transistors:**
  - **10 nm fins are approx. 25% taller and approx. 25% more closely spaced than 14nm**

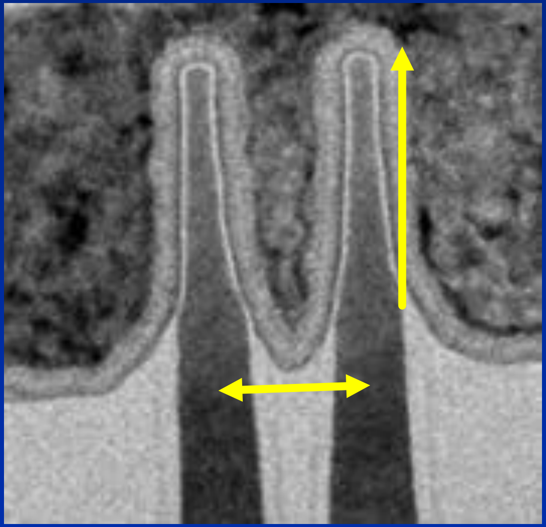
22nm



14nm



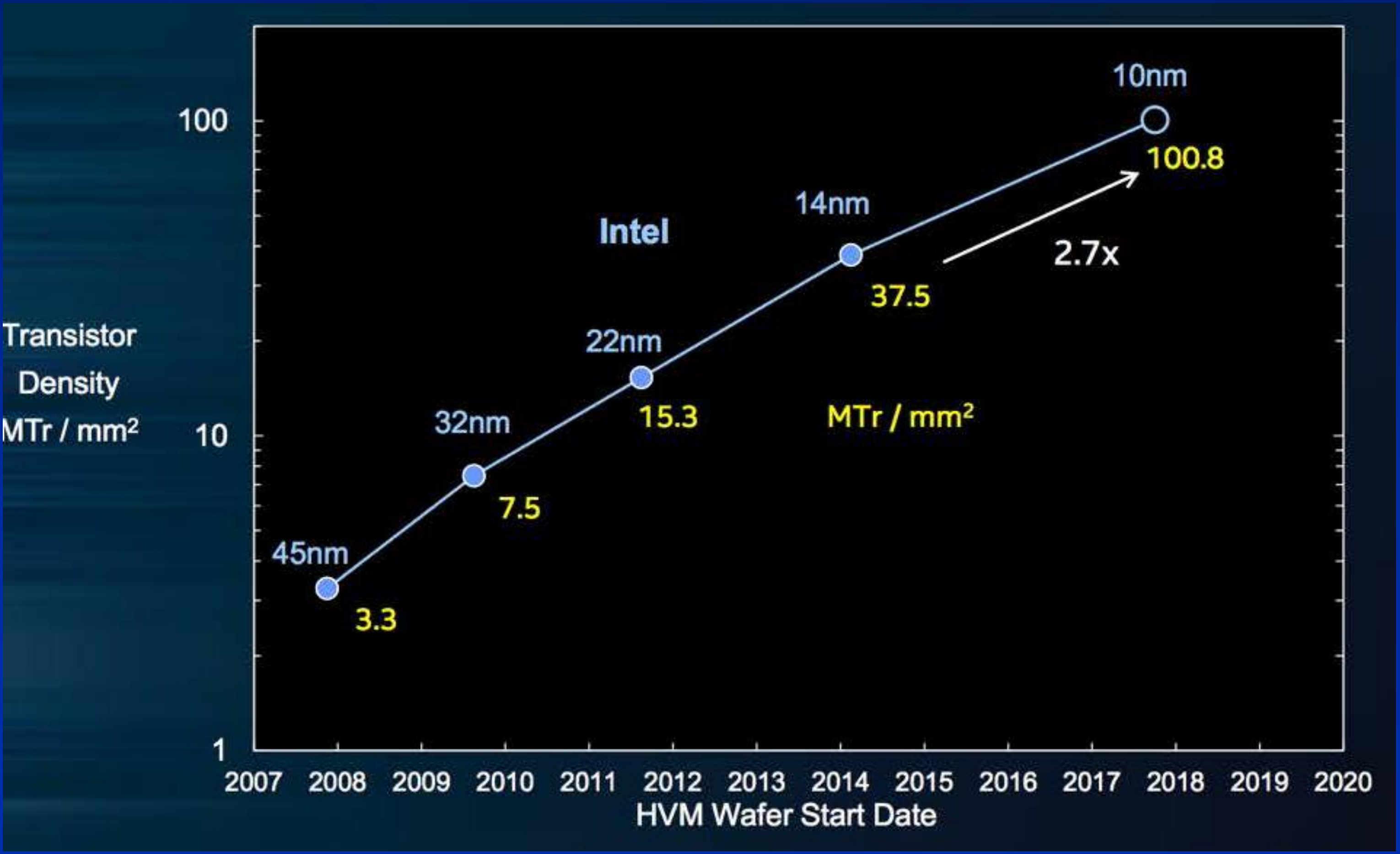
10nm



M. Bohr, "Technology Leadership", Technology and Manufacturing Day, 19 September 2017

How Is It Possible To Follow the Moore Law?(cnt'd)

- □ **10 nm process:** **compared to 14nm, higher transistor density (2,7%), higher performance (25%), and lower power (45%)**



https://newsroom.intel.com/newsroom/wp-content/uploads/sites/11/2017/09/10-nm-icf-fact-sheet.pdf

How Is It Possible To Follow the Moore Law ? (cnt'd)

- ❑ **Intel Optane – announced on March 19th, 2017, available since Aprile 24th, 2017 (16GB, 32GB)**
  - ➢ **Intermediate solution between DRAM and Flash memories**
    - ❖ **DRAM (faster than Flash, less dense than Flash and volatile)**
    - ❖ **Flash – used in current SSD (non volatile, denser than DRAM, slower than DRAM)**

https://newsroom.intel.com/news/intel-introduces-worlds-most-responsive-data-center-solid-state-drive/

non volatile + denser (10X) than DRAM and faster (1000X) than Flash

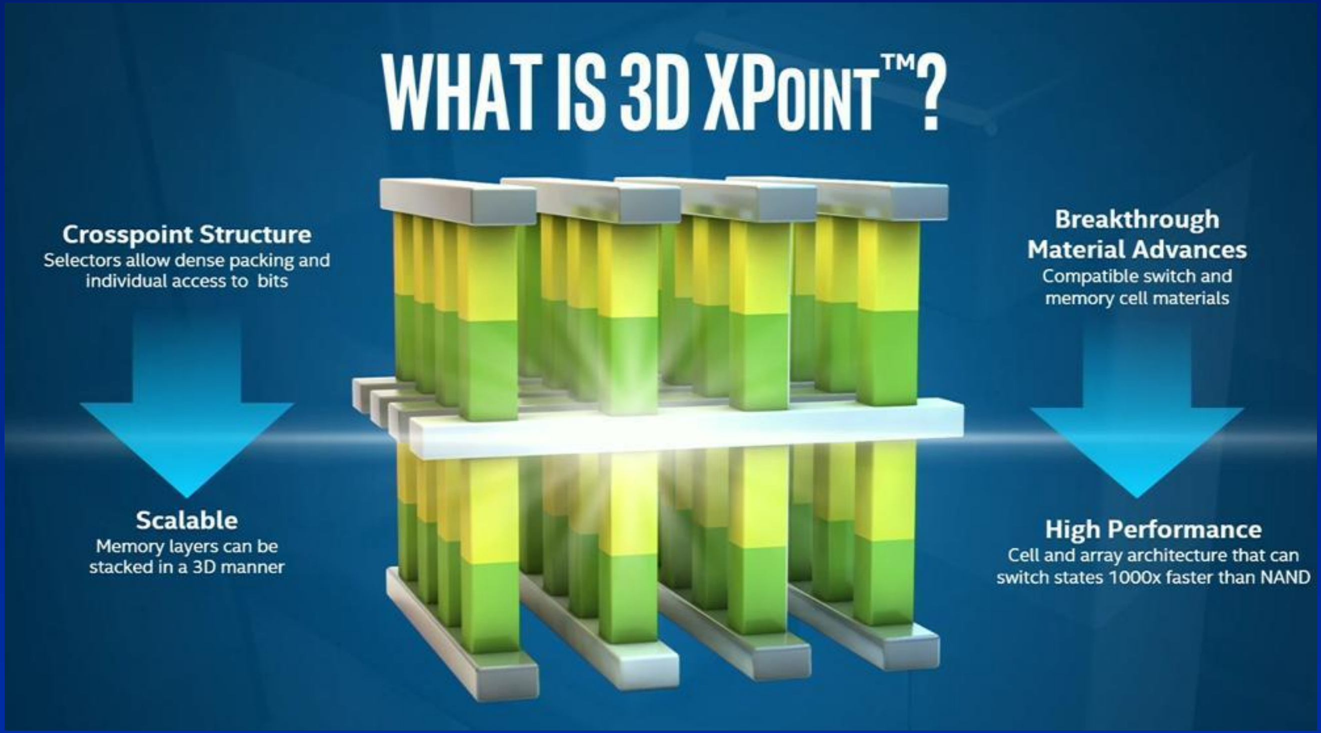
⬇

Technology *"ideal for …devices, applications, services…requiring fast access to large sets of data"*

(http://www.intel.com/content/www/us/en/architecture-and-technology/intel-optane-technology.html)

How Is It Possible To Follow the Moore Law ? (cnt'd)

❑ **Intel Optane– 3D Xpoint Technology:**


WHAT IS 3D XPOINT™?
Crosspoint Structure
Selectors allow dense packing and individual access to bits
Scalable
Memory layers can be stacked in a 3D manner
Breakthrough Material Advances
Compatible switch and memory cell materials
High Performance
Cell and array architecture that can switch states 1000x faster than NAND

http://wccftech.com/intel-storage-roadmap-2017-optane-nand/

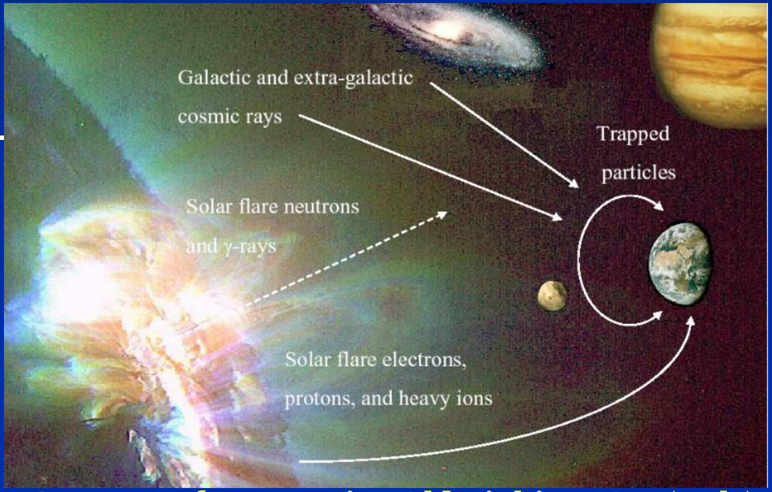
- **Vertical stack (3D) of structures composed by columns (cell, selector) → ↑ density**
- **Each cell can be written/read changing only the voltage sent to the selctor → ↑ speed**

Reliability Challenges in the IoT Era

- Following the Moore law enabled to ↑ integration density, ↑ complexity, and ↑ performance, to arrive to today's IoT, but also:
  - In the Field:
    - ↑ Vulnerability to Transient Faults (TFs) → Soft Errors (SEs)
    - ↑ Likelihood of ageing phenomena (mainly Negative Bias Temperature Instability – NBTI)

⬇

Reliability Challenges



Courtesy of Dr. Monica Alderighi, INAF (Italy)

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- ❑ Reliability Challenges for today's electronics:

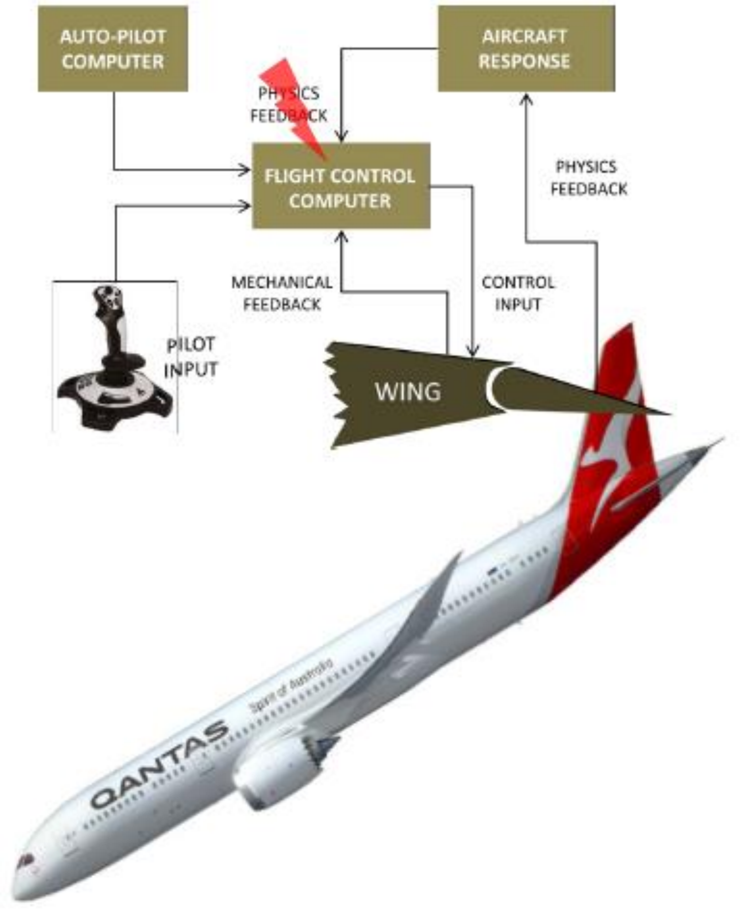
  - ➢↑ Vulnerability to transient faults (TFs) → soft errors (SEs)

  - ➢↑ Likelihood of Aging Phenomena (NBTI)

- ❑ Design Approaches for Reliable electronics.

Reliability Challenges due to TFs and SEs

- □ **TFs and consequent SEs may compromise electronics' correct operation in the field.**



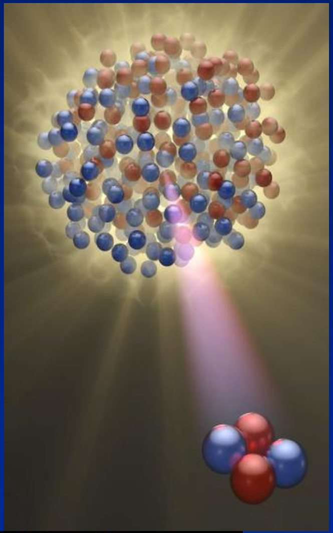
- □ **Example: Unexpected and violent descent of Quantas Flight 72 (Airbus A330-303) caused by particles hitting the flight control computer (October 2008)**

"In-flight upset, 154 km west of Learmonth, WA, 7 Oct. 2008, VH-QPA Airbus A330-303," ATSB Transp. Safety Report - Aviation Occurrence Invest., AO-2008-070, pp. 1 – 313, Dec. 2011.

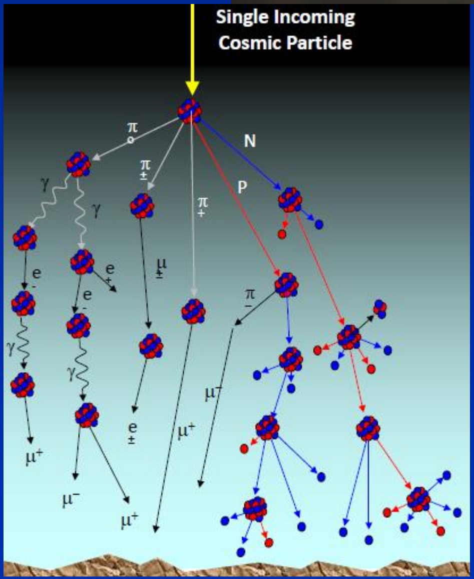
Transient Faults and Soft Errors

- ❑ Undesired voltage fast transition (*spike* or *glitch*) on a circuit node/line.
- ❑ They are generally by:

R. Baumann, «Boron Compounds as a Dominant Source of Alpha Particles in Semiconductor Devices», in Proc. of IEEE Conf. on Reliability Physics Symposium, 1995.



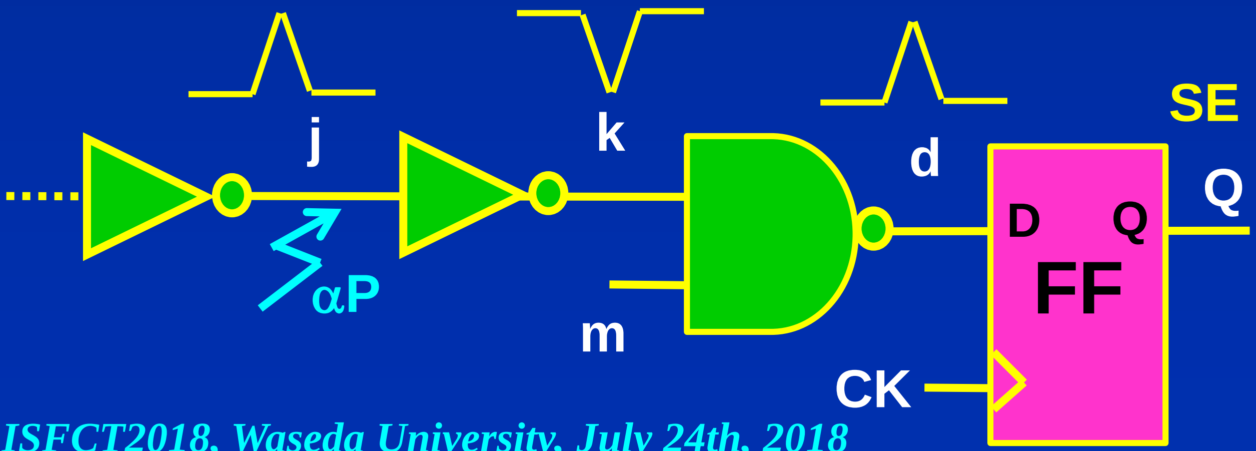
- ➢ Alpha particles: atoms of He that lost the electrons, possibly generated by the radioactive decay of unstable isotopes (e.g., ^{232}Th) present within the packages of electronic circuits
- ➢ Neutrons and protons originated by the collision of Galactic Cosmic Rays (GCRs) and atmosphere atoms (mainly Nitrogen and Oxigen)



J. F. Ziegler, "Terrestrial Cosmic Ray Intensities," IBM J. Res. Develop., Vol. 42(1), p. 125, Jan. 1998.

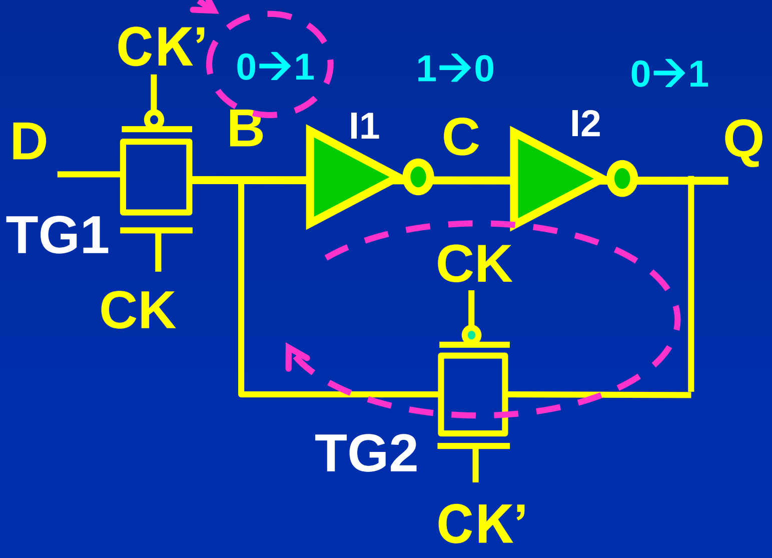
Transient Faults and Soft Errors (cnt’d)

- If the TF affetcs a combinational circuit and is propagated till the input of a sampling element → possible output SE → *Reliability Risks*
- This happens if the TF:
  - Is not electrically filtered out by the gates between j and the FF input
  - Is not logically filtered out (m=1) by the gates between j and the FF input
  - Arrives to the FF input with a spike satisfying the FF’s set-up and hold time conditions wrt the FF sampling instant



Transient Faults and Soft Errors (cnt’d)

- If the TF affetcs a memory element/cell → likely output SE → *Reliability Risks*
- For instance, if the TF hits the internal node B of a standard latch while CK=0 (TG1 OFF, and TG2 ON) :
  - the incorrect voltage value induced by the TF on node B is confirmed by the latch positive feedback loop → logic value of Q changed → SE.



- There is half of the CK period during which TFs can give rise to output SEs → more likely than for TFs affecting the latch input

Outline

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  - ➢ **↑ Vulnerability to transient faults (TFs) → soft errors (SEs)**

  - ➢ **↑ Likelihood of Aging Phenomena (NBTI)**

- ❑ **Design Approaches for Reliable electronics.**

Aging Phenomena - NBTI

- ❑ Negative-Bias Temperature-Instability (NBTI) is the most likely aging effect for current, scaled down Integrated Circuits (ICs)

- ❑ NBTI causes an increase in the absolute value of the V_{th} of pMOS transistors → IC's performance degradation (> 20% in 10 years)

⬇

Signals on time-critical data-paths may violate setup/ hold times of output flip-flops → generation of incorrect outputs → *Reliability Risks*

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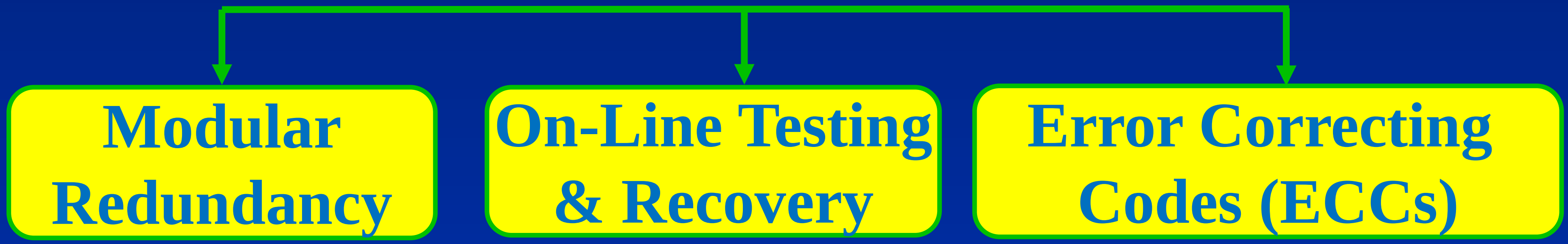
- ➢ ↑ Likelihood of Aging Phenomena (NBTI)

❑ Design Approaches for Reliable electronics.

Design Approaches for Reliable Electronics

- □ Hardware Fault Tolerance (HFT) is successfully adopted to guarantee the system’s correct operation despite the occurrence of TFs and SEs during the in-field operation.
- □ Traditional HFT approaches:



Modular Redundancy

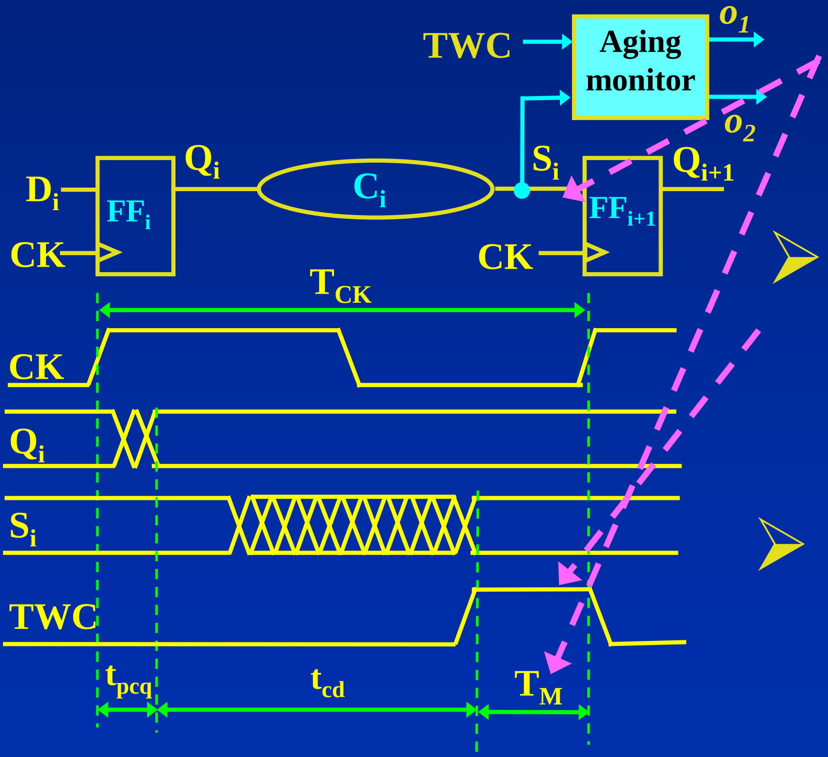
On-Line Testing & Recovery

Error Correcting Codes (ECCs)

- □ Proper aging monitors can be connected to the inputs of FFs at the output of time-critical data-paths → early monitoring of delay effect due to NBTI → possible activation of in-field compensation strategies → system’s correct operation.

Example of Aging Monitors for NBTI

- **Aging monitors** connected to the inputs of the **output FFs of time-critical data-paths ([1, 2]).**
- **Each aging monitor:**
  - Checks the **output** of the data-path C_i (S_i) **during a proper time guardband (T_M)**
  - **Is enabled during T_M only,** by a proper control signal (TWC), which is = 1 only during T_M
  - **Gives** an output **alarm message in case of late transitions of Si during T_M**

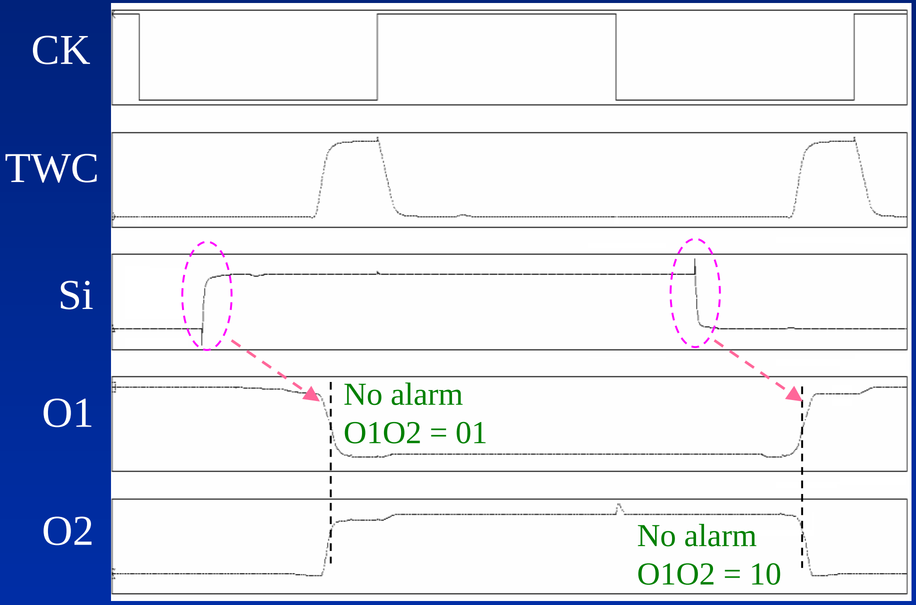


[1] C. Metra, et al., "Self-Checking Monitor for NBTI Due Degradation", in Proc. of IEEE Int. Mixed-Signals, Sensors and Systems Test Workshop (IMS3TW), 2010

[2] C. Metra, et al., "Low Cost NBTI Degradation Detection & Masking Approaches", IEEE Transactions on Computers

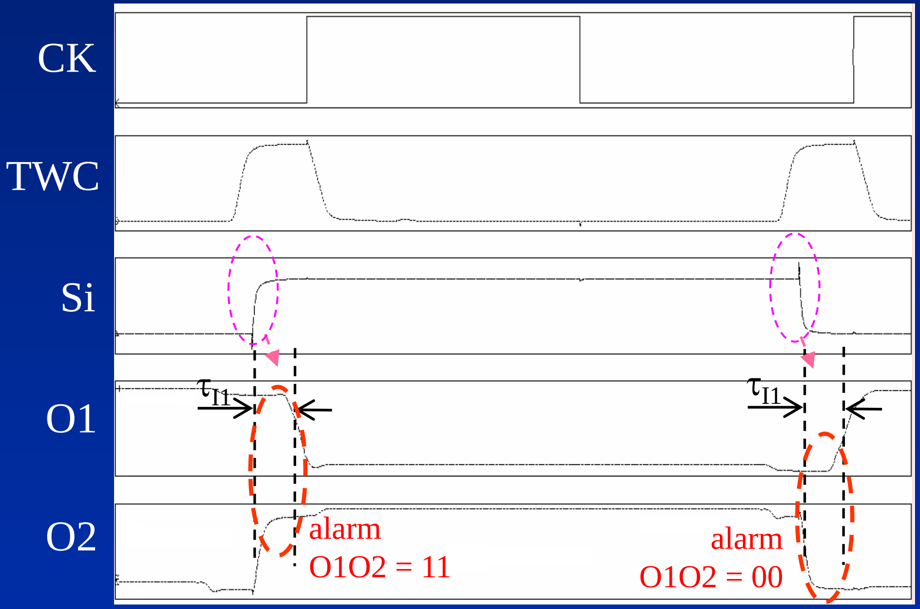
Example of Aging Monitors for NBTI (cnt'd)

- ❑ Case of **no late transition** of S_i while **TWC=1**



- ❑ (O$_1$, O$_2$) = (0,1)/(1,0) → **no alarm message**

- ❑ Case of **late transitions** of S_i while **TWC=1**



- ❑ (O$_1$, O$_2$) = (1,1) or (0,0) → **alarm message**

[2] C. Metra, et al., "Low Cost NBTI Degradation Detection & Masking Approaches", IEEE Transactions on Computers

Example of Aging Monitors for NBTI (cnt’d)

- **Costs (area & power) of the monitor in [2] wrt those in [3, 4]:**

	Area (Sq)	ΔA	Power (μW)	ΔP
Our Monitor [2]	**60**	**-**	**12**	**-**
Monitor in [3]	**78**	**-23%**	**12.2**	**-1.6%**
Monitor in [4]	**62**	**-3.2%**	**15**	**-20%**

$$\Delta A(\%) = 100 \cdot \frac{A_{our} - A_{[3,4]}}{A_{[3,4]}} \qquad \Delta P(\%) = 100 \cdot \frac{P_{our} - P_{[3,4]}}{P_{[3,4]}}$$

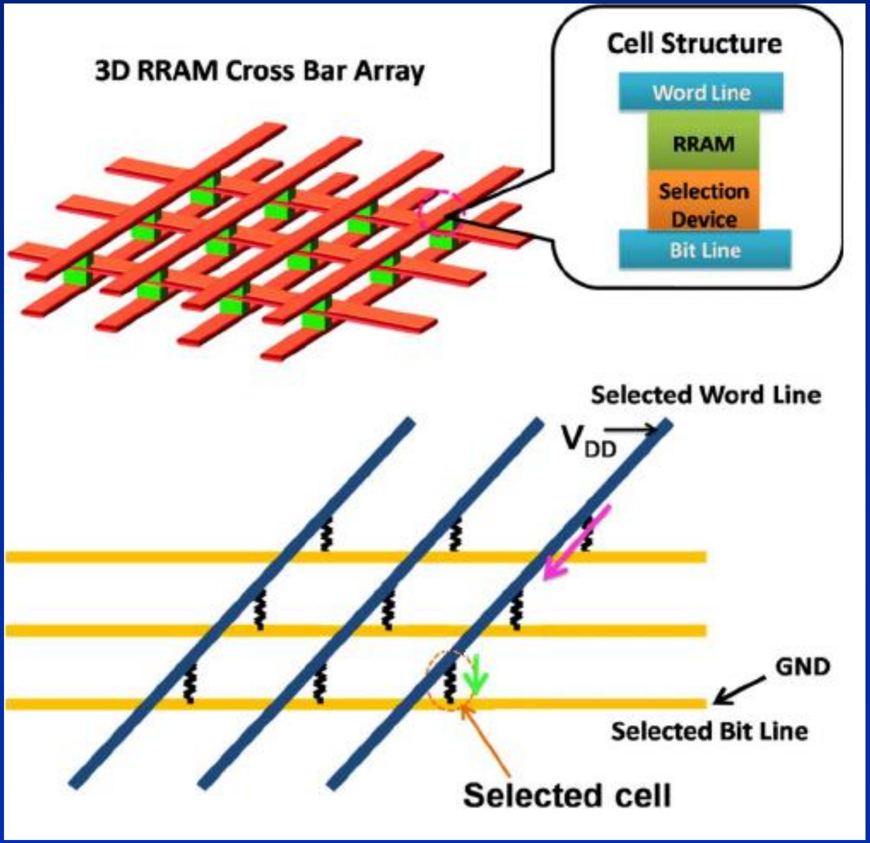
[2] C. Metra, et al., “Low Cost NBTI Degradation Detection & Masking Approaches”, IEEE Transactions on Computers

[3] M. Agarwal et al., “Optimized Circuit Failure Prediction for Aging: Practicality and Promise”, in *Proc. of IEEE Int. Test Conf.*, pp. 1-10, 2008.

[4] A. C. Cabe et al., “Small Embeddable NBTI Sensors (SENS) for Tracking On-Chip Performance Decay“, in *Proc. of Symp. on Quality Electronic Design*, pp. 1-6, 2009.

New Approaches for Reliable Electronics implemented by Emergent Technologies?

- **We have analyzed (by means of Spice simulations) the effects of the most likely faults (i.e., *shorts* and *opens* [2]) affecting the selectors of a *ReRAM* (of size 128x128).**



- **As for opens, our analyses showed that they can alter only the logic value stored in the faulty *ReRAM* cell**

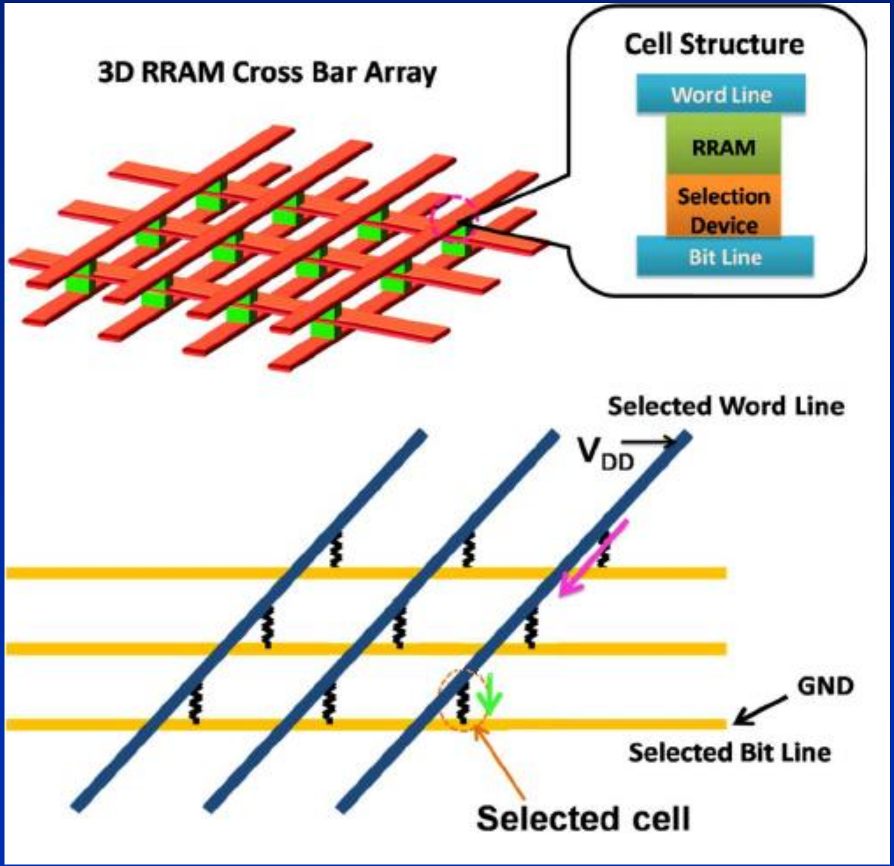
→ Single error → correction by the conventional ECCs

[1] Y. Deng, et al., IEEE Trans. Electron Devices, Feb. 2013.

[2] G. Burr, et al., Journal of Vacuum Science & Tech. B, Jul./Aug. 2014.

New Approaches for Reliable Electronics implemented by Emergent Technologies?cnt'd

- ❑ As for **shorts,** our analyses showed that **they can alter** (due to the huge current through the faulty cell) the **logic value** stored in:



1. The **faulty *ReRAM* cell**, and
2. **Many other cells sharing the same *word line*** as the faulty ***ReRAM***

- ❑ The **# of cells in 2 depends** mainly on the **position of the faulty cell** within the crossbar array, and **it can be > 10.**

→High number of errors →need for alternate solutions to traditional ECCs

[1] *Y. Deng, et al., IEEE Trans. Electron Devices, Feb. 2013.*

Reliability Challenges for High Performance Electronics in the Internet of Things Era

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