System LSI education strategy at Waseda University

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Takeshi Ikenaga
The Graduate School of Information, Production and Systems
Waseda University
Outline

- Introduction of the Grad. School of IPS
  Waseda University

- System LSI educational curriculum
  - Regular and invited lectures

- Subject: “System LSI design”
  - Actual LSI through lectures and exercises
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Graduate School of Information, Production and Systems (IPS)

Just opened in April 1st 2003 at Kitakyushu Science and Research Park
http://www.ips.waseda.ac.jp/

Current status
- 31 professors / associate professors
- 181 master’s or doctoral course students
- 55 students are from overseas and 53 students belong to Ph. D course -
Why Waseda in Kitakyushu?

Tokyo (東京)
Osaka (大阪)
Kitakyushu (北九州)
Fukuoka (福岡)
Hokkaido (北海道)
Beijing (北京)
Seoul (ソウル)
Taiwan (台湾)

500Km 1000Km 1500Km
Three program fields

Information Architecture Field
This field covers the various application of information technology including information representation means through multimedia, information processing means focused on its algorithms, networks for transmitting and processing information, and applications of information process into business management.

Production Systems Field
This field encompasses 21st century oriented production systems that incorporate information technology and covers process engineering and FA system engineering as well as measurement and control engineering being recognized as common technology, and the issue of energy engineering as infrastructure research.

System LSI Field
This fields covers system LSI design; an essential hardware means for supporting the progress of information technology. System LSI applications and its design and verification methodologies are key subjects.

An example of an important production system in the 21st century
System LSI field

- **Advanced education and research for System LSI**
  Largest and best stuffs in System LSI in Japan. Most of all professors have industry background and experience in System LSI.

- **10 professors cover almost all area of system LSI**
  - Vision : Market research and product design
  - Strategy : Architecture design and implementation
  - Design : Methodologies and design tools
  - Tactics : Verification, test and marketing strategy
Faculties and research area

Application Area
Multimedia, Mobile, Ubiquitous

High Level Design and Verification
Takeshi Baba
Takaaki Ikenaga

On-chip Memory and CAM
Satoshi Goto
Shinji Kimura
Tsutomu Yoshihara

Logic Design
Takeshi Yoshimura

Partitioning and Layout
Takahiro Watanabe
Yasuaki Inoue

Integration of Digital / Analog, MEMS, Sensors and Micro Energy
Toshihiko Yoshimasu

Noriyoshi Yamauchi

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Background of faculties

- Satoshi Goto
- Takeshi Yoshimura
- Shinji Kimura
- Takahiro Watanabe
- Noriyoshi Yamauchi
- Toshihiko Yoshimasu
- Takaaki Baba
- Takeshi Ikenaga
- Tsutomu Yoshihara
- Yasuaki Inoue

High Level Design and Verification
- Multimedia, Mobile, Ubiquitous

Logic Design
- Partitioning and Layout

Analog Circuit Design and Simulation
- On-chip Memory and CAM

Integration of Digital / Analog, MEMS, Sensors and Micro Energy
- Analog Circuit Design and Simulation

Digital Designers and Tools
- Toshiba
- Toshiba
- NTT

Multimedia
- NEC
- NAIST
- Panasonic
- Sharp
- Sanyo
- Mitsubishi

Waseda Univ. System LSI International Workshop 20...
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Features of curriculums

- **Regular and invited lectures**
  - Regular lectures (fundamental and advanced subjects) are taught by 10 faculties of IPS and Prof. Ohtsuki (School of Science and Engineering)
  - Invited lectures are taught by guest professors (oversea/domestic) and leading-edge company’s researchers. MEXT invests $5.0 M to Waseda University to run invited lectures (and to support graduate students financially).

- **Theoretical and practical education**
  - Algorithm, architecture and software
  - Voice, motion picture and ubiquitous applications
  - Actual LSI chip design and manufacturing
## Fundamental subjects

<table>
<thead>
<tr>
<th>Subject</th>
<th>Language</th>
<th>Instructor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Digital Signal Processing</td>
<td>E</td>
<td>Baba</td>
</tr>
<tr>
<td>Analog Circuits</td>
<td>E</td>
<td>Yoshimasu</td>
</tr>
<tr>
<td>Introduction System LSI</td>
<td>J</td>
<td>Goto</td>
</tr>
<tr>
<td>Introduction Semiconductor</td>
<td>J</td>
<td>Yoshihara</td>
</tr>
<tr>
<td>Computer Architecture</td>
<td>E</td>
<td>Watanabe</td>
</tr>
<tr>
<td>Software Engineering</td>
<td>J</td>
<td>Yoshimura</td>
</tr>
<tr>
<td>Digital Circuits</td>
<td>J</td>
<td>Kimura</td>
</tr>
<tr>
<td>Numerical Analysis</td>
<td>E</td>
<td>Inoue</td>
</tr>
</tbody>
</table>

- Fall: Fall lectures
- Spring: Spring lectures
- E: English
- J: Japanese

One subject: 12-15 lectures with one hour and a half

*Waseda Univ. System LSI International Workshop 2004*
## Advanced subjects

<table>
<thead>
<tr>
<th>Subject</th>
<th>Orientation</th>
<th>Instructor(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Digital LSI architecture</td>
<td>E</td>
<td>Watanabe</td>
</tr>
<tr>
<td>System LSI architecture</td>
<td>E</td>
<td>Kimura</td>
</tr>
<tr>
<td>Digital LSI design</td>
<td>E</td>
<td>Yamauchi</td>
</tr>
<tr>
<td>System LSI design</td>
<td>E</td>
<td>Ilkenaga</td>
</tr>
<tr>
<td>Multimedia LSI</td>
<td>J</td>
<td>Goto</td>
</tr>
<tr>
<td>Algorithm Design</td>
<td>E</td>
<td>Goto</td>
</tr>
<tr>
<td>Layout design</td>
<td>E</td>
<td>Yoshimura</td>
</tr>
<tr>
<td>Wireless Communication</td>
<td>E</td>
<td>Baba</td>
</tr>
<tr>
<td>Product design</td>
<td>J</td>
<td>Yoshihara</td>
</tr>
<tr>
<td>Communication network</td>
<td>J</td>
<td>Yamauchi</td>
</tr>
<tr>
<td>Interface design</td>
<td>J</td>
<td>Baba</td>
</tr>
<tr>
<td>On chip memory</td>
<td>E</td>
<td>Yoshihara</td>
</tr>
<tr>
<td>Micro Machine</td>
<td>E</td>
<td>Yamauchi</td>
</tr>
<tr>
<td>Transmission circuits</td>
<td>J</td>
<td>Yoshimasu</td>
</tr>
<tr>
<td>High frequency circuits</td>
<td>E</td>
<td>Yoshimura</td>
</tr>
<tr>
<td>System LSI Software</td>
<td>J</td>
<td>Yoshimura</td>
</tr>
<tr>
<td>Design for testability</td>
<td>J</td>
<td>Kimura</td>
</tr>
<tr>
<td>Low Power LSI Design</td>
<td>J</td>
<td>Watanabe</td>
</tr>
<tr>
<td>LSI simulation</td>
<td>J</td>
<td>Inoue</td>
</tr>
<tr>
<td>Analog LSI design</td>
<td>E</td>
<td>Inoue</td>
</tr>
<tr>
<td>Digital Integrated Circuits</td>
<td>J</td>
<td>Ohtsuki</td>
</tr>
</tbody>
</table>

- : Fall
- : Spring
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One subject: 12-15 lectures with one hour and a half
Invited lectures (oversea)

- Prof. Chong-Min Kyung* (KAIST)
  - Current Status and Challenges of SoC Verification for Embedded Systems Market

- Prof. Ernest S. Kuh (UCB)
  - Circuit Simulation Past, Present and Future

- Prof. C. L. Liu* (National Tsing Hua Univ.)
  - Optimization algorithm
  - Computer-aided design of VLSI circuits

* Guest professor of Waseda University
Invited lectures (domestic)

- Prof. Nozomu Togawa* (Univ. Kitakyushu): Dedicated processor design
- Dr. Junji Namiki* (NEC): Technology trend of networking and network processor
- Dr. Masao Nakaya* (Renesas): SoC design methodology
- Dr. Takashi Mitsuhashi* (Toshiba): EDA technology
- Dr. Kazutoshi Wakabayashi (NEC): LSI design from C language
- Dr. Ichiro Kuroda (NEC): Video/Media Processing LSI
- Dr. Toshihiro Hattori (Super H Japan): Embedded Microprocessor
- Dr. Yukiyasu Tsunoo (NEC): Symmetric Key Cipher
- Dr. Kazuhiko Takamizawa (NEC electronics): DFT
- Dr. Masato Edahiro (NEC): On-chip Multiprocessor

* Guest professor of Waseda University
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Purpose of the subject

Master’s course students of system LSI field are expected to design and fabricate two actual LSI’s at least: one in education and the other through research.

“System LSI design”: An actual LSI is designed through lectures and exercises. It’s indispensable to master various system LSI technologies deeply.
Design environment

- 33 PCs and 5 Workstations
- EDA tools (Synopsis, Cadence)
- FPGA evaluation boards
- ASIC Fabrication: VDEC (VLSI design education center)
Syllabus (first half)

- **Top down LSI design methodology**
  - Hardware description language (Verilog HDL), Functional simulation (VCS), Logic synthesis (Design Compiler), Layout (Milkyway/Applo) and design rule check (Dracula)

- **Modeling and Simulation**
  - Combinational Circuits: Multiplexer/Selector, Encoder, Decoder, Priority encode, Comparator, Adder and ALU (Arithmetic Logic Unit)
  - Sequential Circuits: Register file, Counter, Linear Feedback Shift Register and FSM (Finite state machine)
Project #1

- Design target: electric calculator
  - A simple but useful digital system
  - Can learn system design concept and I/O

- Implementation: FPGA board

![Image of FPGA board with labels: Altera FPGA, 7 segment LED x 8, Input ten key x 32]
Result of project #1

Students define a specification of a calculator by themselves and implement it onto the FPGA board.

<table>
<thead>
<tr>
<th></th>
<th>given</th>
<th>attained</th>
</tr>
</thead>
<tbody>
<tr>
<td>Digit</td>
<td>2 (-99 to 99)</td>
<td>3, .., 7 or 8 (-99999999 ~99999999)</td>
</tr>
<tr>
<td>Number</td>
<td>Integer</td>
<td>Floating point or fixed point decimal fraction</td>
</tr>
<tr>
<td>Operator</td>
<td>+, -</td>
<td><em>, /, X^2, 2</em>X, +/-</td>
</tr>
<tr>
<td>Function</td>
<td>CE</td>
<td>Clear, MC, MR, MS, M+, “Error” display</td>
</tr>
</tbody>
</table>
Project #2

- Design target: embedded pipeline processor (MIPS-based 16-bit processor)
  - The most important element in system LSI
  - Can learn hardware, software and their interface
- Implementation: ASIC chip through VDEC
- Linked with "System LSI architecture" and an open seminar on computer architecture.
Specification of processor

- 16 bit five-stage pipeline processor
- 28 RISC-type instructions + user-defined instructions
- Data and operation memories with 8-bit-width address and 16-bit-width data (256 words x 16 bit)
- Eight 16-bit-width general registers (register #1 contains all-0 constant value)
- Three flag registers
- For testing: 16 bit output with 4 bit selection signal
Result of project #2

12 processors in VDEC 0.35 μm 4.9mm²
Chip evaluation

Socket for VDEC Chip (QFP 160)

USB

SRAM

VDEC extension board

ALTERA Stratix

Various I/Os

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## From education to research

<table>
<thead>
<tr>
<th>Programmable</th>
<th>Software</th>
<th>Embedded Processor (e.g. ARM, MIPS, TX, VR, SH, M32R)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Re-Configurable Processor</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Xtensa, MeP, Quick Logic Elixent</td>
</tr>
<tr>
<td></td>
<td>Hardware</td>
<td>Static</td>
</tr>
<tr>
<td></td>
<td></td>
<td>FPGA (e.g. Xilinx, Altera)</td>
</tr>
<tr>
<td></td>
<td>Dynamic</td>
<td>DRP, Quick silver, IPFlex</td>
</tr>
<tr>
<td>Non-Programmable</td>
<td>Long TAT</td>
<td>CBLC</td>
</tr>
<tr>
<td></td>
<td>Short TAT</td>
<td>ISSP, RapidChip, GA</td>
</tr>
</tbody>
</table>

### SoC classification by Prof. GOTO

- Cryptography
- Sensor interface
- Image processing
- Wireless communication
Summary

- **Grad. School of IPS Waseda University**
  - IPS offers unique education and research environment in System LSI

- **System LSI educational curriculum**
  - Regular and invited lectures cover system LSI technologies widely and deeply.

- **“System LSI design”**
  - Experience of designing an actual LSI make a significant contribution to research.