Directional DCT-Correlation with Monotonous Estimation for High Frame-rate and Ultra-low Delay Sub-pixel Location Detection

Background
- Sub-pixel location detection

Target
- Implement high frame rate and ultra-low delay sub-pixel location with FPGA

Challenge
- Redundant calculation for block
- Loss of some information for direction
- Complex fitting function for estimation

Proposal

Proposal1

Proposal2

Proposal3

Evaluation result

Software
Direction X

<table>
<thead>
<tr>
<th></th>
<th>POC(Block)</th>
<th>DCT-sign correlation</th>
<th>P1+P2+P3</th>
</tr>
</thead>
<tbody>
<tr>
<td>AVG</td>
<td>0.17</td>
<td>0.02</td>
<td>0.38</td>
</tr>
<tr>
<td>AVG</td>
<td>0.18</td>
<td>0.12</td>
<td>0.45</td>
</tr>
<tr>
<td>AVG</td>
<td>0.20</td>
<td>0.14</td>
<td>0.49</td>
</tr>
</tbody>
</table>

Conclusion
1. Algorithm with proposal1 improves the result from negative number to positive
2. Implemented algorithm for high frame rate and ultra-low delay sub-pixel location detection achieve the 0.75ms/frame

Hardware performance:
- Processing time: 0.75ms/frame